**EXECUTE SIGNALS: (3 bits)**

**Alu Selector:**

ALU\_SEL = OPCODE(3 downto 0);

**IO/ALU: (1 bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 0 - alu | Rest |
| 1 – io | 01101 |

**Out Selector: (1 bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 0 – ‘Z’ | Rest |
| 1 – Rdst | 01100 |

**ALU operand 2 Selector: (1 bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 0 – Rsrc2 | Rest |
| 1 – IMM | 00010  00101  00110  10010 |

**MEMORY SIGNALS: (7bits)**

**Read/Write Select: (1 bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 0 – Read | 10001  10011  11011  11100 |
| 1 – Write | 10000  10100  11010 |

**Value Selector: (2 bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 00 – “Z” | rest |
| 01 – [Rsrc1] | 10000  10100 |
| 10 – PC | 11010 |
| 11 – FLAGS&PC | INTR |

**Address Selector: (2 bits)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 00 – 1,0 | RST |
| 01 – 3,2 | INTR |
| 10 – EA | 10011  10100 |
| 11 – SP/SP+2 | 10000  10001  11010  11011  11100 |

**(SP ALU) + (SP/SP+2) Selector: (1 bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 0 – ‘+’ and ‘SP+2’ | 10001  11011  11100 |
| 1 – ‘-‘ and ‘SP’ | 10000  11010 |

**SP load: (1 bit)**

|  |  |
| --- | --- |
| **LOAD** | **OPCODE** |
| 0 | Rest of them |
| 1 | 10001  11011  11100  10000  11010 |

**WB SIGNALS: (4 bits)**

**Write Value Select: (2 bits)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 00 – ‘Z’ | rest |
| 01 – MEM | 10001  10011 |
| 10 – EXE | 01001  01010  01011  01101  00111  00000  00001  00010  00011  00100  00101  00110  10010 |
| 11 – [Rsrc1] | Second swap |

**Write Address Select: (2-bit)**

|  |  |
| --- | --- |
| **SEL** | **OPCODE** |
| 00 – Rsrc1 | 01001  01010  01011  01101  00111  00101  00110  10001  1001د0  10011 |
| 01 – Rdst | 00000  00001  00010  00011  00100 |
| 10 – Rsrc2 | Second swap |